CLAIMS

What is claimed is:

1. A method of reading data from a ferroelectric memory cell, the method comprising:

coupling a first ferroelectric cell capacitor terminal to an array bitline;

activating a cell plateline signal to a second ferroelectric cell capacitor terminal to provide a voltage across the ferroelectric cell capacitor;

coupling a first zero cancellation capacitor terminal to the array bitline; and

providing a zero cancellation plateline signal to a second zero cancellation capacitor terminal while the cell plateline signal is activated, the zero cancellation plateline signal comprising a first pre-determined voltage level during a first time period and a second pre-determined voltage level during a second time period, wherein the first voltage level is greater than the second voltage level.

2. The method of claim 1, further comprising sensing a voltage on the array bitline after the second time period.

3. The method of claim 1, wherein the second voltage level is ground and first voltage is Vdd.

4. The method of claim 1, wherein the second voltage level is negative.

5. The method of claim 1, wherein the zero cancellation capacitor is substantially identical to the ferroelectric cell capacitor.

6. The method of claim 1, wherein the zero cancellation capacitor is identical to the ferroelectric cell capacitor.

7. The method of claim 1, further comprising precharging the array bitline to a third pre-determined voltage level before coupling the first ferroelectric cell capacitor terminal to the array bitline.

8. The method of claim 7, wherein the third pre-determined voltage is ground.

9. The method of claim 1, further comprising coupling the first zero cancellation capacitor terminal to a fourth pre-determined voltage level while the second zero cancellation capacitor terminal is coupled to the first pre-determined voltage level before coupling the first zero cancellation capacitor terminal to the array bitline.

10. The method of claim 9, wherein the pre-determined fourth voltage level is ground.

11. The method of claim 1, further comprising precharging the array bitline to a third pre-determined voltage level before coupling the first ferroelectric cell capacitor terminal to the array bitline, further comprising coupling the first zero cancellation capacitor terminal to the third pre-determined voltage level while the second zero cancellation capacitor terminal is coupled to the first pre-determined voltage level before coupling the first zero cancellation capacitor terminal to the array bitline.

12. The method of claim 11, wherein the third pre-determined voltage is ground.

13. The method of claim 1, further comprising precharging the array bitline to a third pre-determined voltage level during pre-charge before coupling the first ferroelectric cell capacitor terminal to the array bitline, further comprising coupling the first zero cancellation capacitor terminal to the array bitline during

the pre-charge while the second zero cancellation capacitor terminal is coupled to the first pre-determined voltage level.

14. The method of claim 13, wherein the third pre-determined voltage is ground.

15. The method of claim 1, further comprising coupling a reference voltage to a complementary array bitline, wherein the reference voltage is zero volts.

16. A method of reading data from a ferroelectric memory cell, the method comprising:

coupling a first ferroelectric cell capacitor terminal to an array bitline;

activating a cell plateline signal to a second ferroelectric cell capacitor terminal to provide a voltage across the ferroelectric cell capacitor;

coupling a first zero cancellation capacitor terminal to the array bitline; and

providing a zero cancellation plateline signal to a second zero cancellation capacitor terminal while the cell plateline signal is activated, the zero cancellation plateline signal comprising a first voltage level during a first time period, a second voltage level during a second time period, and a third voltage level during a third time period, wherein the first and third voltage levels are greater than the second voltage level.

17. The method of claim 16, wherein the first voltage level, the second voltage level and the third voltage level are pre-determined voltage levels.

18. The method of claim 16, wherein the first and third voltage levels are equal.

19. The method of claim 16, wherein the first, second, and third voltage levels are positive.

20. The method of claim 16, further comprising sensing a voltage on the array bitline after the third time period.

21. The method of claim 16, wherein the second voltage level is ground and first voltage is Vdd.

22. The method of claim 16, wherein the second voltage level is negative.

23. The method of claim 16, wherein the zero cancellation capacitor is substantially identical to the ferroelectric cell capacitor.

24. The method of claim 16, wherein the zero cancellation capacitor is identical to the ferroelectric cell capacitor.

25. The method of claim 16, further comprising deactivating the cell plateline signal before sensing the voltage on the array bitline.

26. The method of claim 16, further comprising precharging the array bitline to a pre-determined voltage level before coupling the first ferroelectric cell capacitor terminal to the array bitline.

27. The method of claim 26, wherein the pre-determined voltage level is ground.

28. The method of claim 16, further comprising coupling the first zero cancellation capacitor terminal to a pre-determined voltage level while the second zero cancellation capacitor terminal is coupled to the first voltage level before coupling the first zero cancellation capacitor terminal to the array bitline.

29. The method of claim 28, wherein the pre-determined voltage level is ground.

30. The method of claim 16, further comprising precharging the array bitline to a pre-determined voltage level before coupling the first ferroelectric cell capacitor terminal to the array bitline, further comprising coupling the first zero cancellation capacitor terminal to the pre-determined level while the second zero cancellation capacitor terminal is coupled to the first voltage level before coupling the first zero cancellation capacitor terminal to the array bitline.

31. The method of claim 30, wherein the pre-determined voltage level is ground.

32. The method of claim 16, further comprising precharging the array bitline to a pre-determined voltage level during a pre-charge period before coupling the first ferroelectric cell capacitor terminal to the array bitline, further comprising coupling the first zero cancellation capacitor terminal to the array bitline during the pre-charge period while the second zero cancellation capacitor terminal is coupled to the first voltage level.

33. The method of claim 32, wherein the pre-determined voltage level is ground.

34. A system for reading data using reduced plateline voltages in a ferroelectric memory device, the system comprising:

a zero cancellation capacitor having first and second terminals;

a zero cancellation switching device coupled with the zero cancellation capacitor, the zero cancellation switching device selectively coupling the first zero cancellation capacitor terminal with an array bitline according to a zero cancellation wordline signal; and

a control system coupled with the zero cancellation capacitor and the zero cancellation switching device, the control system providing the zero cancellation wordline signal to the zero cancellation switching device and providing a negative pulse of a pre-determined magnitude to the second zero cancellation capacitor terminal while a cell plateline signal is activated to create a voltage across a target ferroelectric cell capacitor.

35. The system of claim 34, wherein the control system provides a zero cancellation plateline signal to the second zero cancellation capacitor terminal while the cell plateline signal is activated, the zero cancellation plateline signal comprising a first pre-determined voltage level during a first time period and a second pre-determined voltage level during a second time period, wherein the first pre-determined voltage level is greater than the second pre-determined voltage level.

36. The system of claim 35, wherein the zero cancellation plateline signal further comprises a third pre-determined voltage level during a third time period after the second time period, wherein the third pre-determined voltage level is greater than the second pre-determined voltage level.

37. The system of claim 36, wherein the first and third pre-determined voltage levels are equal.

38. The system of claim 36, wherein the first, second, and third pre-determined voltage levels are positive.

39. The system of claim 34, further comprising a zero cancellation discharge switching device coupled with the zero cancellation capacitor, the zero cancellation discharge switching device selectively coupling the first zero cancellation capacitor terminal to a pre-determined voltage level according to a zero cancellation discharge signal from the control system.

40. The system of claim 39, wherein the pre-determined voltage level is ground.

41. The system of claim 34, wherein the zero cancellation capacitor is a ferroelectric capacitor.

42. A ferroelectric memory device, comprising:

an array of ferroelectric memory cells arranged in rows and columns, the cells individually comprising at least one ferroelectric cell capacitor having first and second terminals and at least one cell transistor adapted to selectively couple the first cell capacitor terminal to one of a pair of array bitlines associated with an array column according to an array wordline, wherein rows of the memory cells are coupled with a corresponding wordline;

a zero cancellation system coupled with the array, the zero cancellation system comprising a plurality of zero cancellation circuits individually coupled with the array bitlines, the zero cancellation circuits individually comprising a zero cancellation capacitor having first and second terminals, and a zero cancellation switching device coupled with the zero cancellation capacitor, the zero cancellation switching device selectively coupling the first zero cancellation capacitor terminal with an array bitline according to a zero cancellation wordline signal; and

a control system coupled with the zero cancellation capacitor and the zero cancellation switching device, the control system providing the zero cancellation wordline signal to the zero cancellation switching device and providing a negative pulse of a pre-determined magnitude to the second zero cancellation capacitor terminal while a cell plateline signal is activated to provide a voltage across a target ferroelectric cell capacitor.

43. The ferroelectric memory device of claim 42, wherein the control system provides a zero cancellation plateline signal to the second zero

cancellation capacitor terminal while the cell plateline signal is activated, the zero cancellation plateline signal comprising a first pre-determined voltage level during a first time period and a second pre-determined voltage level during a second time period, wherein the first pre-determined voltage level is greater than the second pre-determined voltage level.

44. The ferroelectric memory device of claim 43, wherein the zero cancellation plateline signal further comprises a third pre-determined voltage level during a third time period after the second time period, wherein the third pre-determined voltage level is greater than the second voltage level.

45. The ferroelectric memory device of claim 44, wherein the first and third pre-determined voltage levels are equal.

46. The ferroelectric memory device of claim 44, wherein the first, second, and third pre-determined voltage levels are positive.

47. The ferroelectric memory device of claim 42, further comprising a zero cancellation discharge switching device coupled with the zero cancellation capacitor, the zero cancellation discharge switching device selectively coupling the first zero cancellation capacitor terminal to a pre-determined voltage level according to a zero cancellation discharge signal from the control system.

48. The system of claim 47, wherein the pre-determined voltage level is ground.

49. The ferroelectric memory device of claim 42, wherein the zero cancellation capacitor is a ferroelectric capacitor.